



# ***Intel<sup>®</sup> IXDP425 / IXCDP1100 Development Platform***

**Quick Start Guide**

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***January 2005***



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## Revision History

Date	Revision	Description
January 2005	006	Updated for Microsoft* Windows* CE.
July 2004	005	Edited for clarity.
March 2004	004	Added information regarding IXP420 network processor variants.
December 2003	003	Removed Packing List section. Updated Inspection section.
September 2003	002	Updated related documentation location, other minor updates.
June 2003	001	Initial release of this document.

## 1.0 Purpose

This document contains instructions for unpacking, setting up, and starting the Intel® IXDP425 / IXCDP1100 Development Platform (KIXDP425BD) and a brief introduction to the components. Sections 5.0, 6.0, and 7.0 are for informational purposes. Setup of the IXDP425 / IXCDP1100 platform begins in Section 8.0. For more detailed information, see the *Intel® IXDP425 / IXCDP1100 Development Platform User's Guide*.

## 2.0 Applicable Documents and Revisions

The documents referenced below may be obtained online unless noted otherwise.

**Table 1. Reference Documents**

Title	Document Number	Location
<i>Intel® IXDP425 / IXCDP1100 Development Platform User's Guide</i>	273743	Documentation Web Page <sup>†</sup>
<i>Intel® IXDP425 / IXCDP1100 Development Platform Specification Update</i>	253527	Intel Representative
<i>Intel® IXP400 Software Release 1.3 Software Release Notes</i>	N/A	Software Web Page <sup>††</sup>
<i>Intel® IXDP425 / IXCDP1100 Development Platform Boot-Loader Flash Conversion Guide</i>	253201	Documentation Web Page <sup>†</sup>
<i>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update</i>	252702	Intel Representative
<i>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet</i>	252479	Documentation Web Page <sup>†</sup>
<i>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual</i>	252480	Documentation Web Page <sup>†</sup>
<i>Intel® IXP400 Software Specification Update</i>	273795	Intel Representative
<i>Intel® IXP400 Software Programmer's Guide</i>	252539	Documentation Web Page <sup>†</sup>

<sup>†</sup> This document is available at: <http://www.intel.com/design/network/products/npfamily/docs/ixp4xx.htm>

<sup>††</sup> This document is available at: <http://www.intel.com/design/network/products/npfamily/ixp425swr1.htm>

## 3.0 Known Issues

Known issues with the IXDP425 / IXCDP1100 platform are described in the *Intel® IXDP425 / IXCDP1100 Development Platform Specification Update*. Silicon and software errata are described in the *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update* and the *Intel® IXP400 Software Specification Update*.

## **4.0 Inspection**

Unpack the contents of the box. After all the components are unpacked, verify that all the items listed in packing list are present. The packing list is included in the Readme file shipped with the kit. Inspect each item for any visible damage. Inspect the cable connectors to ensure that none of the pins are bent or damaged. If any item is damaged or missing, see [Section 11.0, “Technical Support”](#).

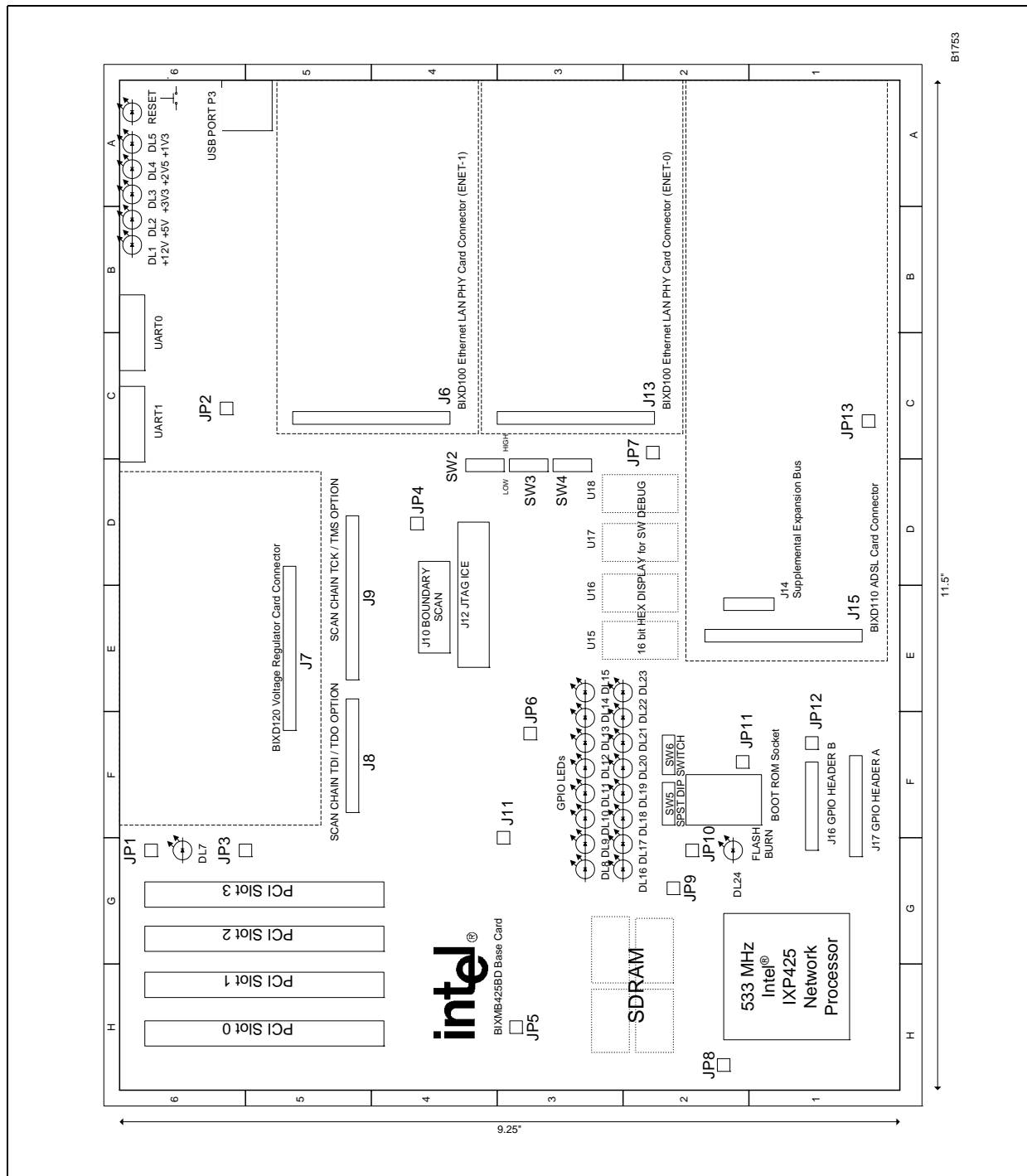
## **5.0 Intel® IXDP425 / IXCDP1100 Development Platform Overview**

The Intel® IXDP425 / IXCDP1100 Development Platform consists of the BIXMB425BD Base Card, two BIXD100 Ethernet Cards, one BIXD110 ADSL CPE card, and one BIXD120 Voltage Regulator card, that all plug into the base card. The IXDP425 / IXCDP1100 platform ships with a 533-MHz IXP425 network processor. This platform can be used for development with the Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor.

### **5.1 BIXMB425BD Base Card Component Placement Diagram**

[Figure 1](#) shows the main components of the BIXMB425BD Base Card and the location of the BIXD100, BIXD110, and BIXD120 connectors; some of these components are referred to later in this document.

Figure 1. Top View: BIXMB425BD Component Placement Diagram



For reference, Table 2 lists the jumpers that are shown in Figure 1 and provides a description of each jumper and its default setting.

**Table 2. Jumper Setting Descriptions for the BIXMB425BD Base Card**

Reference	Description	Default Setting
JP1	GND	No Shunt
JP2	GND	No Shunt
JP3	PCI Clock – Allow 66-MHz operation through the PCI slot. (1-2) Run at 33 MHz on the PCI slot (2-3)	Shunt 1-2
JP4	GND	No Shunt
JP5	GND	No Shunt
JP6	Expansion bus clock – 33-MHz external oscillator (1-2) or GPIO15 (2-3)	Shunt 1-2
JP7	GND	No Shunt
JP8	cPCI Clock – Allow 66 MHz operation through the compact PCI slot. (1-2) Run at 33 MHz on the compact PCI slot (2-3)	No Shunt
JP9	+3.3 V Power Measurement	No Shunt
JP10	GND	No Shunt
JP11	Flash Boot Address – 0000 0000h (1-2) 0080 0000h (2-3)	Shunt 1-2
JP12	UTOPIA-2 input and output clock – 33 MHz Enabled: (1-2), Disabled (2-3)	Shunt 1-2
JP13	+1.3 V Power Measurement	No Shunt
J11	PCI Clock – GPIO (1-2) 33-MHz external oscillator (3-4) 66-MHz external oscillator (5-6)	Shunt 1-2

## 6.0 BIXMB425BD Base Card Hardware Settings

This section is used to show default settings that may need to be changed to start using the development platform. “[Verifying Jumper Settings](#)” on page 13 steps you through the process of verifying these settings are set for your development environment.

For reference, a complete description of all the settings are described in the *Intel® IXDP425 / IXCDP1100 Development Platform User’s Guide*.



## 6.1 Processor Frequency Setting

To set the processor frequency, the switches on SW2 (Figure 1, C4) should be set as described in Table 3. The silk screen near the switch is labeled 'Low' and 'High'.

**Table 3. Processor Frequency Settings**

Part in Processor Socket	Desired Frequency	SW2[8: 7: 6] Setting
IXP425BD, IXC1100BD, or IXP420BD	533 MHz	[High: High: High] <b>(default)</b>
	400 MHz	[Low: Low: High]
	266 MHz	[Low: High: High]
IXP420BC, IXP425BC or IXC1100BC	400 MHz	[High: High: High]
	266 MHz	[Low: High: High]
IXP420BB, IXP421BB, IXP422BB, IXP425BB, or IXC1100BB	266 MHz	[High: High: High]

## 6.2 Configuring PCI Operation to 33 or 66 MHz

The platform is shipped with 33-MHz PCI operation. The configuration settings for 33/66 MHz PCI Operation are shown in Table 4. The PCI slots available during 33/66 MHz operation are shown in Table 5.

**Table 4. Jumper Setting Descriptions for 33/66 MHz Operation**

Reference	33-MHz Operation Setting	66-MHz Operation Setting
SW4 Clock Speed of the PCI Interface	SW4.5 'Low'	SW4.5 'High'
JP3 PCI Slot Configuration –	'Shunt 2-3'	'Shunt 1-2'
J11 PCI Clock –	'Shunt 3-4'	'Shunt 5-6'

**Table 5. PCI Slots During 33/66 MHz Operation**

PCI Slot	33-MHz Operation	66-MHz Operation
0	33-MHz capable	66-MHz capable
1	33-MHz capable	66-MHz capable
2	33-MHz capable	(Should not be populated)
3	33-MHz capable	(Should not be populated)

## 7.0 Card Definitions

The BIXD100 Ethernet PHY Card, BIXD110 ADSL Card and BIXD120 Voltage Regulator Card are all built compatible to the connectors available on the BIXMB425BD Base Card. This section gives brief introductions to the cards. [Section 8.1](#) steps you through a process to verify that the settings are correct.

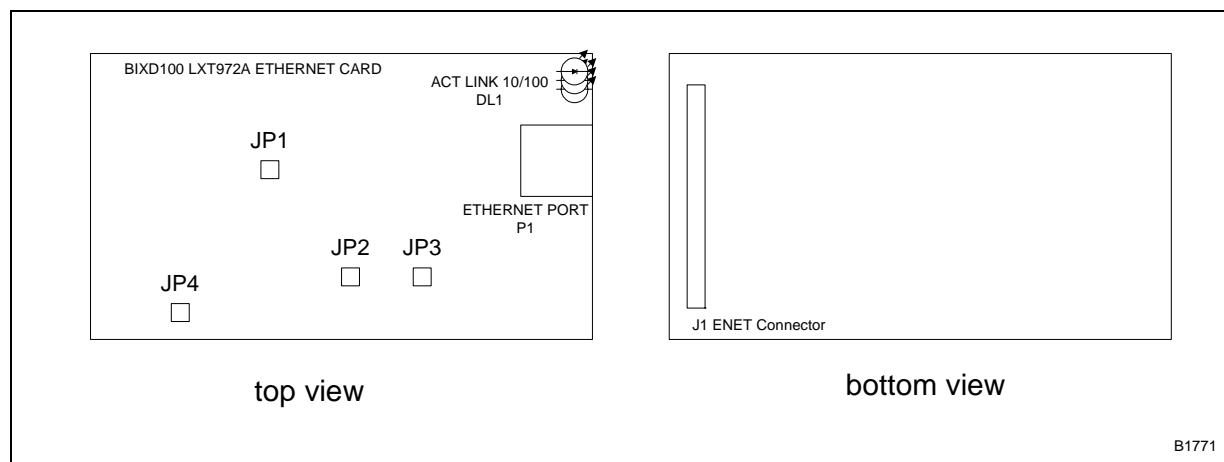
### 7.1 BIXD100 Ethernet PHY Card

#### 7.1.1 Introduction

The BIXD100 Ethernet PHY cards are compatible to J6 ([Figure 1, C4](#)) or J13 ([Figure 1, C2](#)) connectors on BIXMB425BD Base Card.

The BIXD100 maps its own address to BIXMB425BD Base Card memory map. JP2 ([Figure 2](#)) on the BIXD100 card defines the address. The setting on JP2 must be opposite on each card if both BIXD100 Ethernet PHY cards are plugged in. (See [Table 6](#).)

**Figure 2. BIXD100 Ethernet Card Component Placement Diagram**



**Table 6. Jumper Setting Descriptions for the BIXD100 Ethernet Card**

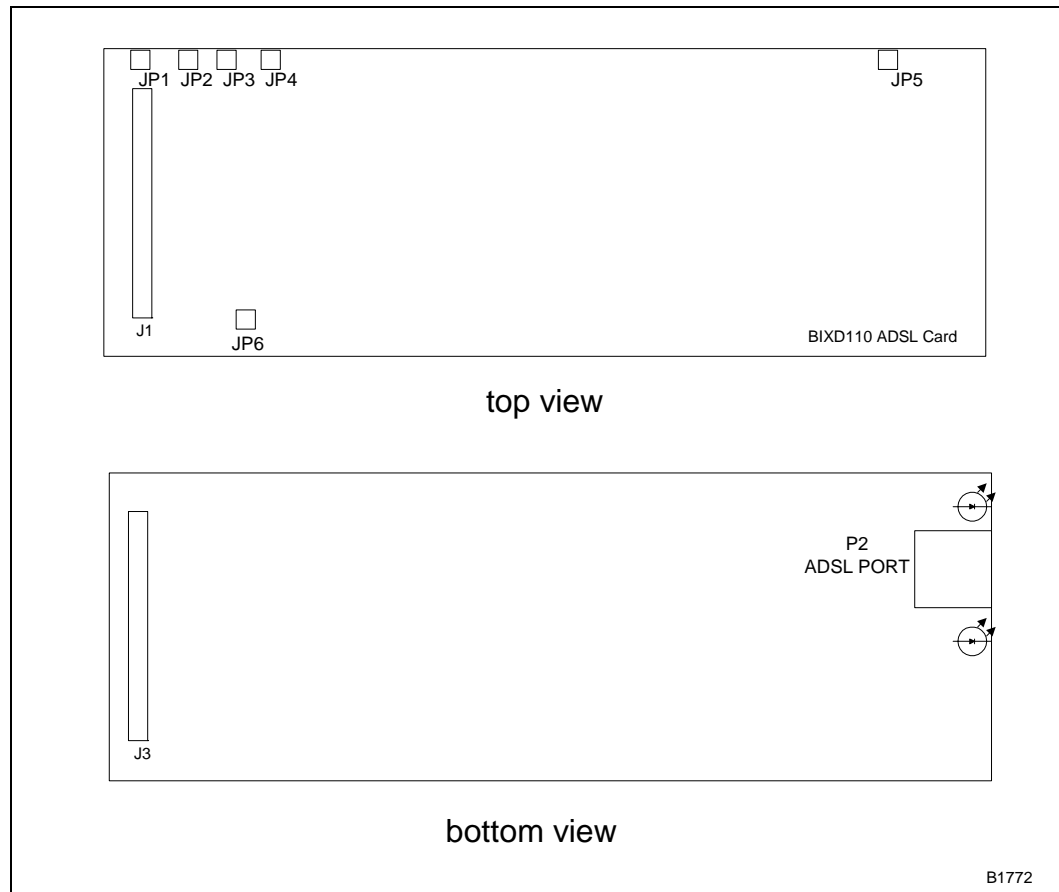
Reference	Description	Default Setting
JP1	GND	No Shunt
JP2	Defines the address of the BIXD100 Card	ENet-0 – Shunt 2-3 ENet-1 – Shunt 1-2
JP3	GND	No Shunt
JP4	GND	No Shunt

## 7.2 BIXD110 ADSL Card Definition

### 7.2.1 Introduction

The BIXD110 ADSL PHY Card is compatible with the UTOPIA-2 Module Connector, J15 (Figure 1, E1.)

**Figure 3. BIXD110 ADSL Card Component Placement Diagram**



**Table 7. Jumper Setting Descriptions for the BIXD110 ADSL Card**

Reference	Description	Default Setting
JP1	Defines the address of the BIXD110 Card	Shunt 2-3
JP2	Defines the address of the BIXD110 Card	Shunt 2-3
JP3	Defines the address of the BIXD110 Card	Shunt 2-3
JP4	GND	No Shunt
JP5	GND	No Shunt
JP6	GND	No Shunt

## 7.2.2 Unplugged BIXD110 ADSL Card or Unused UTOPIA-2 Interface Instructions

Some developers may not need the ADSL card, such as those developing with the Intel® IXP420 Network Processor, Intel® IXP422 Network Processor, or Intel® IXC1100 Control Plane Processor. If the BIXD110 ADSL card is not plugged into the UTOPIA-2 connector and the UTOPIA-2 signals are not used, change JP12 (Figure 1, F1) on the BIXMB425BD Base Card to shunt 2-3 to disable the UTOPIA-2 clock.

## 7.3 BIXD120 Voltage Regulator Card

### 7.3.1 Introduction

The BIXMB425BD Base Card receives its power through the BIXD120 Voltage Regulator Card. The BIXD120 generates voltages on the board from power supplied through the A/C power supply. The BIXD120 provides +12 V, +5 V, +3V3 (+3.3 V), +2V5 (+2.5 V), -64 V, and -32 V to the BIXMB425BD. DL1 (+12 V), DL3 (+5 V), DL4 (+3.3 V), DL2 (+2.5 V) light up in a red color after the voltages are regulated.

Figure 4. BIXD120 Voltage Regulator Card Component Placement Diagram

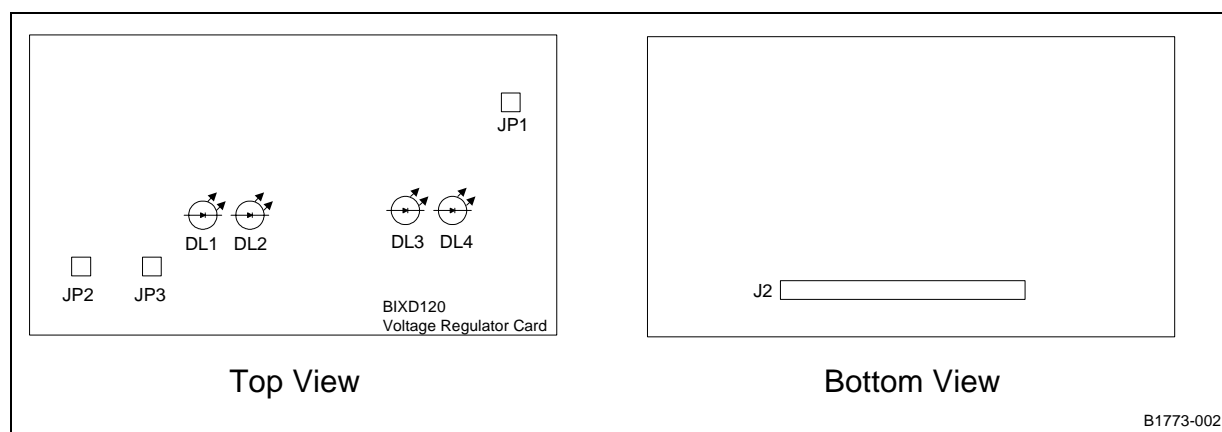


Table 8. Jumper Setting Descriptions for the BIXD120 Voltage Regulator Card

Reference	Description	Default Setting
JP1	Force_On. Must be shunted when BIXD120 is not connected to the BIXMB425BD Base Card.	No Shunt
JP2	-32 V Power Measurement	No Shunt
JP3	-64 V Power Measurement	No Shunt

## 8.0 Preparing the Platform for Use

After unpacking the board and before powering on the board, follow the steps below.

### 8.1 Verifying Jumper Settings

To prepare the Intel® IXDP425 / IXCDP1100 Development Platform for use, refer to [Figure 1](#) for the location of the jumpers and verify the settings are set for your operating environment. The label near the jumper also shows the various options available.

1. Expansion bus clock –
  - 33-MHz external oscillator, shunt 1-2 on JP6 ([Figure 1, C4](#)),  
or
  - GPIO15 selectable, shunt 2-3
2. Flash Address Select – To boot from 0000 0000h, shunt 1-2 on JP11 ([Figure 1, F1](#))
3. PCI operation –
  - 33-MHz PCI operation set SW4 ([Figure 1, D3](#)) switch 5 'Low', shunt 2-3, shunt 2-3 on JP3 ([Figure 1, F3](#)), and shunt only 3-4 on J11 ([Figure 1, F3](#).)  
or
  - 66-MHz PCI operation set SW4 ([Figure 1, D3](#)) switch 5 'High', shunt 2-3, shunt 1-2 on JP3 ([Figure 1, F3](#)) and shunt only 5-6 on J11 ([Figure 1, F3](#).)
4. On the BIXD100 Ethernet Cards –
  - ENET-1 (card closest to the UART ports): shunt 1-2 on JP2 ([Figure 2](#))
  - ENET-0 (card closest to the ADSL Card): shunt 2-3 on JP2 ([Figure 2](#)),
5. If you plan to unplug the BIXD110 ADSL Card, see “[Unplugged BIXD110 ADSL Card or Unused UTOPIA-2 Interface Instructions](#)” on page 12.
6. Set the processor frequency accordingly, 533 MHz is the default setting; if you would like to set a different frequency see “[Processor Frequency Setting](#)” on page 9.

### 8.2 Hardware Setup

To prepare the Intel® IXDP425 / IXCDP1100 Development Platform for use, follow these steps:

1. Install the Intel® Pro/100 + Adapter Card into PCI slot 0 or PCI slot 1 and connect a cross-over Ethernet cable between the PCI Ethernet card and host system.  
  
*Note:* An alternative option is to use a straight Ethernet cable and go through a hub.
2. Connect the serial cable between COM1 on the host system to UART0 for Windows\* CE developers or Linux\* developers (default Boot ROM on Flash) or to UART1 for VxWorks developers of the BIXMB425BD Base Card. [Table 9](#) shows the UART serial communication values.

**Table 9. UART Communications Configuration**

Parameter	Linux* Value	VxWorks* Value	Windows* CE Values
Port	UART0	UART1	UART0
Bits per Second	115,2000	9,600	38,800
Data Bits	8	8	8
Parity	None	None	None
Stop Bit	1	1	1
Flow Control	None	None	None

## 9.0 Starting the Platform

To start the platform, follow these steps:

1. Verify that the power switch on the A/C power supply is in the off position.
2. Connect power to the IXDP425 / IXCDP1100 platform power connector on the BIXD120 Voltage Regulator Card.
3. Power on the board by flipping the black switch on the A/C power supply. Verify Power Rail LEDs illuminate red on the BIXMB425 Base Card (+12 V, +5 V, +3V3 (+3.3 V), +2V5 (+2.5 V), and +1V3 (+1.3 V)) and BIXD120 Voltage Regulator Card (+12 V, +2V5 (+2.5 V), +5 V, and +3V3 (+3.3 V)).
4. To verify the board booted properly, see that the four hex displays (Figure 1, E2/D2) read 0001.

## 10.0 Operating the Platform

The software release notes are intended to guide the user through software installation and setup of the host computer, and can be found at the following Web site:

<http://www.intel.com/design/network/products/npfamily/ixp425swr1.htm>.

In the “Software Available” section of the above Web site, select the latest software release; for example, “Intel® IXP400 Software v 1.4”. Then click the link for the release notes; for example, “1.4 release notes”.

Linux developers should follow the instructions in the software release notes.

Windows\* CE and VxWorks developers should begin by switching to the flash part with the appropriate Boot-Loader -- VxWorks 5.5 Boot-Loader or Windows\* CE eBoot. (These flash parts are provided in a black box with a white label that shipped with your platform. Follow the *Intel® IXDP425 / IXCDP1100 Development Platform Boot-Loader Flash Conversion Guide* for detailed instructions on this process.) Then follow the instructions in the software release notes.

Further detailed instructions about using the IXDP425 / IXCDP1100 platform are provided in the *Intel® IXDP425 / IXCDP1100 Development Platform User's Guide*.



## **11.0      Technical Support**

If any of the contents are missing or if you have any questions, contact your local Intel representative.

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